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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/522,057	04/25/2005	Huan nan Ma	E1734-00007	2070

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4 VENTURE, SUITE 250
IRVINE, CA 92618

EXAMINER	
KAO, WEI PO ERIC	
ART UNIT	PAPER NUMBER
2416	

NOTIFICATION DATE	DELIVERY MODE
09/16/2009	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

jcpatents@sbcglobal.net
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Advisory Action Before the Filing of an Appeal Brief	Application No.	Applicant(s)	
	10/522,057	MA ET AL.	
	Examiner	Art Unit	
	WEI-PO KAO	2416	

--The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

THE REPLY FILED 26 August 2009 FAILS TO PLACE THIS APPLICATION IN CONDITION FOR ALLOWANCE.

1. ☒ The reply was filed after a final rejection, but prior to or on the same day as filing a Notice of Appeal. To avoid abandonment of this application, applicant must timely file one of the following replies: (1) an amendment, affidavit, or other evidence, which places the application in condition for allowance; (2) a Notice of Appeal (with appeal fee) in compliance with 37 CFR 41.31; or (3) a Request for Continued Examination (RCE) in compliance with 37 CFR 1.114. The reply must be filed within one of the following time periods:
   a) ☒ The period for reply expires 3 months from the mailing date of the final rejection.
   b) ☐ The period for reply expires on: (1) the mailing date of this Advisory Action, or (2) the date set forth in the final rejection, whichever is later. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of the final rejection.
   Examiner Note: If box 1 is checked, check either box (a) or (b). ONLY CHECK BOX (b) WHEN THE FIRST REPLY WAS FILED WITHIN TWO MONTHS OF THE FINAL REJECTION. See MPEP 706.07(f).

Extensions of time may be obtained under 37 CFR 1.136(a). The date on which the petition under 37 CFR 1.136(a) and the appropriate extension fee have been filed is the date for purposes of determining the period of extension and the corresponding amount of the fee. The appropriate extension fee under 37 CFR 1.17(a) is calculated from: (1) the expiration date of the shortened statutory period for reply originally set in the final Office action; or (2) as set forth in (b) above, if checked. Any reply received by the Office later than three months after the mailing date of the final rejection, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

NOTICE OF APPEAL

2. ☐ The Notice of Appeal was filed on _____. A brief in compliance with 37 CFR 41.37 must be filed within two months of the date of filing the Notice of Appeal (37 CFR 41.37(a)), or any extension thereof (37 CFR 41.37(e)), to avoid dismissal of the appeal. Since a Notice of Appeal has been filed, any reply must be filed within the time period set forth in 37 CFR 41.37(a).

AMENDMENTS

3. ☐ The proposed amendment(s) filed after a final rejection, but prior to the date of filing a brief, will not be entered because
   (a) ☐ They raise new issues that would require further consideration and/or search (see NOTE below);
   (b) ☐ They raise the issue of new matter (see NOTE below);
   (c) ☐ They are not deemed to place the application in better form for appeal by materially reducing or simplifying the issues for appeal; and/or
   (d) ☐ They present additional claims without canceling a corresponding number of finally rejected claims.
   NOTE: _____. (See 37 CFR 1.116 and 41.33(a)).
4. ☐ The amendments are not in compliance with 37 CFR 1.121. See attached Notice of Non-Compliant Amendment (PTOL-324).
5. ☐ Applicant's reply has overcome the following rejection(s): _____.
6. ☐ Newly proposed or amended claim(s) _____ would be allowable if submitted in a separate, timely filed amendment canceling the non-allowable claim(s).
7. ☒ For purposes of appeal, the proposed amendment(s): a) ☐ will not be entered, or b) ☒ will be entered and an explanation of how the new or amended claims would be rejected is provided below or appended.
   The status of the claim(s) is (or will be) as follows:
   Claim(s) allowed: _____.
   Claim(s) objected to: _____.
   Claim(s) rejected: 1-5.
   Claim(s) withdrawn from consideration: _____.

AFFIDAVIT OR OTHER EVIDENCE

8. ☐ The affidavit or other evidence filed after a final action, but before or on the date of filing a Notice of Appeal will not be entered because applicant failed to provide a showing of good and sufficient reasons why the affidavit or other evidence is necessary and was not earlier presented. See 37 CFR 1.116(e).
9. ☐ The affidavit or other evidence filed after the date of filing a Notice of Appeal, but prior to the date of filing a brief, will not be entered because the affidavit or other evidence failed to overcome all rejections under appeal and/or appellant fails to provide a showing a good and sufficient reasons why it is necessary and was not earlier presented. See 37 CFR 41.33(d)(1).
10. ☐ The affidavit or other evidence is entered. An explanation of the status of the claims after entry is below or attached.

REQUEST FOR RECONSIDERATION/OTHER

11. ☒ The request for reconsideration has been considered but does NOT place the application in condition for allowance because: See Continuation Sheet.
12. ☐ Note the attached Information *Disclosure Statement*(s). (PTO/SB/08) Paper No(s). _____
13. ☐ Other: _____.

/Ricky Ngo/
Supervisory Patent Examiner, Art Unit 2416

/Wei-po Kao/
Examiner, Art Unit 2416

Continuation of 11. does NOT place the application in condition for allowance because:

In response to the remark on pages 2 and 3:
In response to the entire content of the remarks, in particular that "Shiragaki does not disclose that "fourth, a bypass will be set up after low layer processing module detecting high layer processing module encountering the trouble, so as to isolate the high layer processing module encountering the trouble" as recited in claim 1" because "Firstly, layer B cannot be informed that layer A remains in a failed state after receiving notice 203 and 208, what layer B can be informed is that layer A has started failure recovery and layer B earl switch the main signal. The layer B cannot be informed whether layer A encounters a failure or not. Secondly, that a bypass is set up cannot be concluded. Layer A just stops failure recovery, which does not mean that layer A has encountered a failure. Layer A still may communicate with other layer. Though layer B can switch the main signal to complete the failure recovery, the person ordinary skill in the art cannot conclude that layer A is isolated and bypassed," the examiner respectfully disagrees. According to passage [0177], it states the following: "… a case where failures are detected in both layers will be examined below" (referring to figure 3 and paragraphs [0178-0188]). The passage clearly teaches that there are multiple failures detected in both layers. In another word, the passage suggests that each layer encounters at least one failure. Such suggestion can also see proof from the figure 3, where element 201 shows a failure being detected by the A layer and element 202 shows a failure being detected by the B layer. As a result, Shiragaki's teaching of figure 3 and paragraphs [0178-0188], discloses a mechanism to set up a bypass when B layer detects A layer encountering a failure and therefore isolate the A layer. In particular, the passage [0182] states the following: "At this time, the layers communicate with each other the fact that failure recovering has started as failure recovery starting notices 203 and 204 using the inter A-B layer failure recovery information communication terminal and processing units 103 and 104." It is clear that the notices 203 and 204, not only communicate the fact that failure recovering has started on the respective layers, but also indicate the fact that the failure has been detected by the respective layers. Furthermore, considering the example presented by the Shiragaki in paragraph [0185-0188]: after the A layer and the B layer have detected the failures and started the recovery processes, the B layer, namely the lower layer, sends the notice 207 to the A layer, namely the higher layer to reserve the path. Upon receiving the notice 207, the higher layer stops the recovery process (indicating that the higher layer still is experiencing failure) and sends the notice 208 to the lower layer so the lower layer has the right the transmit the data traffic. In conclusion, the higher layer, which is still encountering a trouble, is isolated and the data traffic is switched by the lower layer, thus bypassing the higher layer.

In response to the remark on pages 3 and 4:
In response to the entire content of the remarks, in particular that "Pierson was cited to teach that "second, …" as recited in claim 1. However, Pierson fails to teach such features too. Therefore, Pierson cannot cure the deficiencies of Shiragaki.
Pierson's technical solution is related to data transmission between two networks, namely ATM and SONET. For example, according to column 10 lines 14-26, the path of the data is ATM transmitter à SONET transmitter à ATM switch à SONET receiver à ATM receiver. The technical solution of claim 1 is related to data transmission between high layer processing module and low layer processing module of one multi-layer communication equipment. The high layer processing module extracts and inserts high layer service of the said node from low layer transmission so that the service between the upstream node and downstream node of the multi- layer communication equipment can keep unchanged. For the reasons discussed above, claim 1 is patentable over Shiragaki and Pierson. Claims 3-5 depend from claim 1 and, thus, are also patentable over Shiragaki and Pierson for at least the same reasons," the examiner respectfully disagrees. Column 10 lines 14-26 states the following: "In one embodiment, ATM network 101 is implemented as a high speed fiber optic network. In this embodiment, ATM transmitter 760 sends the data cell to SONET transmitter 780. SONET is an ATM bearing physical standard designed for high speed fiber optic networks. SONET is described as an example ATM bearing physical signal standard and is not intended to limit the present invention. SONET transmitter 780 loads the data cell into a SONET frame and sends the SONET signal over the ATM network to the destination ATM switch (ATM switch 105 or ATM switch 110). At the destination ATM switch, SONET receiver 770 unloads the data cell from the SONET frame and sends the data cell to ATM receiver 750." In addition, Pierson also discloses the following: "Asynchronous Transfer Mode (ATM) is an asynchronous type of communications protocol based on a cell-switched network. It is designed to be carried over the emerging fiber optical network, called the Synchronous Optical NETwork (SONET), although it can be carried over almost any communications link" (column 2 lines 31-36) and "FIG. 7 illustrates a block diagram of the T1/ATM interface at ATM switches 105 and 110 in FIG. 1, where switches 105, 110 would be located in different nodes in ATM network 101" (column 9 lines 13-16). Based on the above disclosure, the examiner respectfully suggests that the Applicants may have misinterpreted the passage, column 10 lines 14-26. Most importantly, Pierson teaches that the ATM network 101 as shown in the figure 1 is implemented over a high speed fiber optic network of a SONET. Together the network 101 forms an ATM over SONET high speed network, which is a commonly known layered network with ATM as a higher layer and SONET as a lower layer. Therefore, the Applicants' suggestion that Pierson's teaching exhibits a non-layered network (an ATM network-to-SONET network transmission) is improper especially when the figure 7 shows that the SONET transmitter 780 and SONET receiver 770 are merely components of an ATM switch. In conclusion, the examiner respectfully asserts that the claim 1 is not patentable over Siragaki and Pierson.

In response to the remark on page 4:
In response to the entire content of the remarks, in particular that "Conoscenti cannot cure the deficiencies of Shiragaki and Pierson as discussed in eormeetion with claim 1. Therefore, claim 1 is patentable over Shiragaki, Pierson, and Conoseenti. Claim 2 depends on claim 1 and, thus, is also patentable over Shiragaki, Pierson, and Conoscenti for at least the same reasons discussed above. Further more, Conoscenti does not specifically teach the above features recited in claim 2. Conoscenti discloses that "the cells pass through the ATM processing elements of the network without changing the VPI/VCI values" (see column 4, lines 46-62). It can be seen that the VPI/VCI values remain constant throughout the network. In the technical solution of claim 2, the VPI/VCI remains unchanged when a transparent virtual path connection is set up for the service passing the high layer processing module of the said node. That is to say, the VPI/VCI remains unchanged under special condition but does not remain unchanged throughout the network. It is not obvious for the person skill in the art to obtain the technical solution of claim 2 combining what Shiragaki, Pierson and Conoscenti disclose," the examiner

respectfully disagrees. Column 5 lines 33-35 states the following: "… the ATM cells may ride in synchronous slots on a high-speed tiem division multiplexed media, such as a SONET optical fiber." In another word, Conoscenti's invention is capable of perform in an ATM over SONET network as the combined teaching of Shiragaki and Pierson. Therefore, the examiner respectfully asserts that the combination of Shiragaki, Pierson and Conoscenti teaches the claimed limitations in the presented claim 2..